DIGITAL SYSTEM DESIGN LABORATORY

III Semester: ECE

Course Code	Category	Hours / Week			Credits	Maximum Marks		
		L	T	P	C	CIA	SEE	Total
AECC06	Core	0	0	2	1	30	70	100
Contact Classes: Nil	Tutorial Classes: Nil	Practical Classes: 28				Total Classes: 28		

Prerequisite: There are no prerequisites to take this course.

I. COURSE OVERVIEW:

The laboratory strives in researching the logic design and related fields. Digital logic testers are used to provide students with practical training and familiarize themselves with the various functions of logic gates and using integrated components to complete circuitry functions and develop an interest in digital logic and enlighten them in the abilities of deduction. The lab allows students to conduct actual gate-level experiments to increase student interest and develop skills to design digital gates using VHDL.

II. COURSE OBJECTIVES:

The students will try to learn:

I. Design of combinational circuits using Verilog Hardware Description Language.
II. Implementation of Sequential circuits using Verilog Hardware Description Language.
III. Demonstration of different case studies for Verilog.

III. COURSE SYLLABUS:

Week – 1: REALIZATION OF A BOOLEAN FUNCTION

Design and simulate the HDL code to realize three and three variable Boolean functions

Week – 2: DESIGN OF DECODER AND ENCODER

Design and simulate the HDL code for the following combinational circuits

a. 3 to 8Decoder
b. 8 to 3 Encoder (With priority and without priority)

Week – 3: DESIGN OF MULTIPLEXER AND DEMULTIPLEXER

Design and simulate the HDL code for the following combinational circuits

a. Multiplexer
b. De-multiplexer

Week – 4: DESIGN OF CODE CONVERTERS Verification of V-I characteristics of Zener diode and perform

Design and simulate the HDL code for the following combinational circuits

a. 4 - Bit binary to gray code converter
b. 4 - Bit gray to binary code converter Comparator

Week – 5: FULL ADDER AND FULL SUBTRACTOR DESIGN MODELING

Write a HDL code to describe the functions of a full Adder and full subtractor using three modeling styles

Week – 6: DESIGN OF 8-BIT ALU

Design a model to implement 8-bit ALU functionality

Week – 7: HDL MODEL FOR FLIP FLOPS

Write HDL codes for the flip-flops - SR, D, JK, T

Week – 8: DESIGN OF COUNTERS

Write a HDL code for the following counters

a. Binary counter
b. BCD counter (Synchronous reset and asynchronous reset)

Week – 9: HDL CODE FOR UNIVERSAL SHIFT REGISTER
Design and simulate the HDL code for universal shift register

Week – 10: HDL CODE FOR CARRY LOOK AHEAD ADDER
Design and simulate the HDL code for carry look ahead adder

Week – 11: HDL CODE TO DETECT A SEQUENCE
Write a HDL code to detect the sequence 1010101 and simulate the code

Week – 12: CHESS CLOCK CONTROLLER FSM USING HDL
Design a chess clock controller FSM using HDL and simulate the code.

Week – 13: TRAFFIC LIGHT CONTROLLER USING HDL
Design a traffic light controller using HDL and simulate the code

Week – 14: ELEVATOR DESIGN USING HDL CODE
Write HDL code to simulate Elevator operations and simulate the code

V. REFERENCE BOOKS:

1. SamirPalnitkar, "Verilog HDL: "A Guide to Digital Design and Synthesis", Sun Microsystems Press, 2nd Edition, 2003.
2. T.R. Padmanabhan, B. Bala Tripura Sundari, "Design Through Verilog HDL", New Jersey, Wiley- IEEE Press, 2009.
3. Zainalabedin Navabi, "Verilog Digital System Design", TMH, 2nd Edition, 2008.
4. PeterMinns, IanElliott, "FSM-based Digital Design using Verilog HDL", John Wiley & Sons Ltd.

VI. WEB REFERENCES:

1. https://inst.eecs.berkeley.edu/~cs150/fa06/Labs/verilog-ieee.pdf
2. http://www.asic-world.com/www.sxecw.edu.in